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10/675,706	01/09/2004	Young-Min Shin	8021-168 (SS-17883-US)	6305

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F. CHAU & ASSOCIATES, LLC
130 WOODBURY ROAD
WOODBURY, NY 11797

EXAMINER	
FLORES, LEON	
ART UNIT	PAPER NUMBER
2611	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,706	SHIN, YOUNG-MIN	
	Examiner	Art Unit	
	LEON FLORES	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-15 and 17-20* is/are rejected.

7)☒ Claim(s) *6 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims (1-20) have been considered but are moot in view of the new ground(s) of rejection.

Response to Remarks

Applicant asserts that, *"the cited art, taken alone or in combination, fails to teach or suggest that the slave circuit is reset by a reset control signal that is generated outside of the master circuit and the slave circuit".*

The examiner respectfully disagrees. In regards to Shin, the circuit that generates the reset signal is within the master circuit. (See fig. 5 of applicant's disclosure) And the circuit that generates the reset circuit (In Shin) is exactly the same circuit as applicant. (See fig. 6-7 & ¶ 12) In Regards to Jarvis, when S0 (slave time value) is not equal to M0 (master time value) the time value of S0 is set (reset) to M0, which was sent by a circuit in the master circuit.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,577,692 B1 Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following reason:

Application	Patent
Re claim 1, A digital system comprising: a master circuit, which includes a circuit to detect clock delay, receives a system reset signal, and generates output data, an output clock signal with which the output data is synchronized, and a reset control signal which responds to the system reset signal; and a slave circuit in signal communication with the master circuit, where the slave circuit is reset in response to the reset control signal using the system reset signal that is generated outside of	Re claim 1, A digital system comprising: a master circuit having a clock forwarding circuit for generating a first clock signal; and a slave circuit coupled to the master circuit for generating a second clock signal synchronized with the first clock signal; wherein said clock forwarding circuit receives the second clock signal, detects a delay between the first and second clock signals, and sets initial data load/unload parameters of the master circuit based on the detected delay, the clock forwarding circuit using the initial date load/unload parameters to generate the first clock signal.

the master circuit and the slave circuit, receives the output clock signal and the output data, and sends to the master circuit an input clock signal as a feedback signal of the output clock signal and input data that is synchronized with the input clock signal, wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input clock signal, and loads and unloads the input data in response to a variable initialization parameter corresponding to the detected delay.	

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate these obvious variations into the instant application, as taught by the patent, for the benefit of detecting delays.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. **Claims (1-2) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944) in view of Jarvis.(US Patent 5,918,040)**

Re claim 1, Shin discloses a digital system comprising: a slave circuit in signal communication with the master circuit, receives the output clock signal and the output data, and sends to the master circuit an input clock signal as a feedback signal of the output clock signal and input data that is synchronized with the input clock signal. (See fig. 1 & paragraph 3)

But the reference of Shin fails to explicitly teach that wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal, detects a delay between the output clock signal and the input

clock signal, and loads and unloads the input data in response to a variable initialization parameter corresponding to the detected delay.

However, the reference of Shin does teach that wherein the circuit to detect clock delay generates the reset control signal in response to the system reset signal or an internal reset signal (See fig. 7 & paragraph 16), detects a delay between the output clock signal and the input clock signal (See fig. 7 & paragraph 16), and loads and unloads the input data in response to a variable initialization parameter corresponding to the detected delay. (See figs 6 & 7 & paragraph 16)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the benefit of achieving synchronization.

The reference of Shin discloses the limitation as claimed above, except he fails to explicitly teach a master circuit, which includes a circuit to detect clock delay, receives a system reset signal, and generates output data, an output clock signal with which the output data is synchronized, and a reset control signal which responds to the system reset signal; and where the slave circuit is reset in response to the reset control signal.

However, Jarvis does. (See fig. 2 & col. 3, line – col.4, line 44) Jarvis discloses a synchronization process between a master circuit and a slave circuit.

Taking the combined teachings of Shin and Jarvis as a whole, it would have been obvious to one of ordinary skills in the art to incorporate these features into the system of Shin, in the manner as claimed and as taught by Jarvis, for the benefit of

achieving synchronization.

Re claim 2, the combination of Shin and Jarvis further teaches that wherein the internal reset signal is a clock signal generated when detected delays are not identical to one another. (In Shin, see fig. 7: 198 & paragraph 16-19)

2. **Claims (3, 5, 10, 12-13, 18, 20) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944)**

Re claim 12, Shin discloses a method of detecting clock delay comprising: detecting a delay between an output clock signal and an input clock signal and automatically generating a variable initialization parameter corresponding to the detected delay if the detected delays are identical to one another (See fig. 6: 150 & 180 & ¶ 15 & fig. 7 & ¶ 16); continuously detecting the delay until the detected delays are identical to one another (See fig. 7 & ¶ 16); and loading and unloading input data in response to the automatically generated variable initialization parameter. (See fig. 6: 150 & fig. 7 & ¶ 16)

But the reference of Shin fails to explicitly teach generating a reset control signal in response to the system reset signal or the internal reset signal that is generated outside of a master circuit and a slave circuit, if the detected delays are not identical to one another.

However, the reference of Shin does teach a control unit which reset the clock generation machine and the detecting unit when all the detected delay is not in

agreement. (See fig. 7: 198 & ¶ 16 “the reset signal is generated in the clock forwarding circuit")

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the benefit of resetting the clock generation machine and the detecting unit.

Re claim 13, the reference of Shin further discloses that wherein step (a) further comprises: detecting and outputting a delay between the output clock signal and the input clock signal (See fig. 6: 180 & ¶ 15-16); respectively latching most significant bits and least significant bits of the delays outputted in step (a1) (See fig. 7 & ¶ 18); and comparing the most significant bits and the least significant bits outputted in step (a2), outputting one of the most significant bits and one of the least significant bits as the initial parameters, and outputting a first signal at a first level if all most significant bits and least significant bits are respectively identical to one another, or outputting the first signal at a second level if all most significant bits and least significant bits are not respectively identical to one another. (See fig. 7 & ¶s 16-19)

Re claim 18, the reference of Shin further discloses that wherein the internal reset signal is generated when the detected delays are not identical to one another. (See fig. 7: the output of element 196 & ¶s 16-19)

Claim 3 is a system claim corresponding to method claim 12. Hence, the steps

in method claim 12 would have necessitated the elements in system claim 3 as claimed. Therefore, claim 2 has been analyzed and rejected w/r to claim 12 above.

Claim 5 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 5 as claimed. Therefore, claim 5 has been analyzed and rejected w/r to claim 12 above.

Claim 10 is a system claim corresponding to method claim 18. Hence, the steps in method claim 18 would have necessitated the elements in system claim 10 as claimed. Therefore, claim 10 has been analyzed and rejected w/r to claim 18 above.

Claim 20 is a system claim corresponding to method claim 12. Hence, the steps in method claim 12 would have necessitated the elements in system claim 20 as claimed. Therefore, claim 20 has been analyzed and rejected w/r to claim 12 above.

3. **Claims (4 & 14) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944)**

Re claim 14, the reference of Shin fails to explicitly teach that wherein step (b) is characterized by generating the reset control signal for resuming step (a) in response to the first signal if one of the detected delays is not identical to other detected delays and resuming step (a) by N-bit free running until the detected delays are identical to one another.

However, the reference of Shin does teach a control unit which reset the clock generation machine and the detecting unit when all the detected delay is not in agreement. (See fig. 7 & ¶s 16-19)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the benefit of resetting the clock generation machine and the detecting unit.

Claim 4 is a system claim corresponding to method claims 13 & 14. Hence, the steps in method claims 13 & 14 would have necessitated the elements in system claim 3 as claimed. Therefore, claim 4 has been analyzed and rejected w/r to claims 13 & 14 above.

4. **Claims (7 & 15) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944)**

Re claim 15, the reference of Shin further discloses that wherein step (b) further comprises: (b1) generating an internal reset signal in response to the first signal and a predetermined clock signal (See fig. 7: the output of element 196 & paragraphs 16-19); and (b3) performing N-bit free running in response to the first signal and generating an N-bit free running signal. (See fig. 7: 197 & ¶s 16-19)

But the reference of Shin fails to explicitly teach (b2) receiving the system reset signal or the internal reset signal, and generating the reset control signal.

However, the reference of Shin does teach a control unit which reset the clock

generation machine and the detecting unit when all the detected delay is not in agreement. (See fig. 7 & ¶s 16-19)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the benefit of resetting the clock generation machine and the detecting unit.

Claim 7 is a system claim corresponding to method claim 15. Hence, the steps in method claim 15 would have necessitated the elements in system claim 7 as claimed. Therefore, claim 7 has been analyzed and rejected w/r to claim 15 above.

5. **Claims (9 & 17) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944)**

Re claim 17, the reference of Shin fails to explicitly teach that wherein the output clock signal is outputted from a predetermined master circuit, the input clock signal is outputted from a predetermined slave circuit, and the input clock signal is a feedback clock of the output clock signal.

However, in another embodiment, the reference of Shin does teach that the output clock signal is outputted from a predetermined master circuit, the input clock signal is outputted from a predetermined slave circuit, and the input clock signal is a feedback clock of the output clock signal. (See fig. 1 & ¶ 3)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the

benefit of achieving synchronization between two transceivers.

Claim 9 is a system claim corresponding to method claim 17. Hence, the steps in method claim 17 would have necessitated the elements in system claim 9 as claimed. Therefore, claim 9 has been analyzed and rejected w/r to claim 17 above.

6. **Claims (11 & 19) are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin Eibin. (hereinafter Shin) (JP2001/051944)**

Re claim 19, the reference of Shin fails to explicitly teach that wherein the reset control signal is generated when the system reset signal or the internal reset signal is activated.

However, the reference of Shin does teach a control unit which reset the clock generation machine and the detecting unit when all the detected delay is not in agreement. (See fig. 7 & ¶s 16-19)

Therefore, it would have been obvious to one of ordinary skills in the art to incorporate this feature into the system of Shin, in the manner as claimed, for the benefit of resetting the clock generation machine and the detecting unit.

Claim 11 is a system claim corresponding to method claim 19. Hence, the steps in method claim 19 would have necessitated the elements in system claim 11 as claimed. Therefore, claim 11 has been analyzed and rejected w/r to claim 19 above.

Allowable Subject Matter

7. Claims (8 & 16) are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEON FLORES whose telephone number is (571)270-1201. The examiner can normally be reached on Mon-Fri 7-5pm Alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/L. F./
Examiner, Art Unit 2611
July 12, 2008

/David C. Payne/

Supervisory Patent Examiner, Art Unit 2611